Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (previously presented): An integrated electrical circuit, comprising:

a plurality of structure planes including at least one element structure plane;

electrically active elements disposed on said at least one element structure plane;

a first insulation layer disposed above said at least one element structure plane;

said first insulation layer having first contact holes disposed therein, and said first contact holes being filled with a metal;

a second insulation layer disposed above said first insulation layer;

said second insulation layer having second contact holes disposed therein and filled with electrical connecting leads, and said second contact holes being further filled with copper in a whole-area manner;

connection pieces disposed underneath said electrical connecting leads and above said first contact holes;

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impeding and preventing a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in a region having said first contact holes formed therein, said blocker layer disposed between said first insulation layer and said second insulation layer; and

said connection pieces being made of aluminum and covering said first contact holes and contacting said connection leads, and said connection pieces being covered by said second insulation layer.

Claim 2 (previously presented): The integrated electrical circuit according to claim 1, including a diffusion barrier for impeding a diffusion of copper disposed at at least one of

a surface of said first contact holes and said connection pieces.

Claim 3 (original): The integrated electrical circuit according to claim 1, wherein said electrical connecting leads have a copper content that is at least 10 percent by weight.

Claim 4 (original): The integrated electrical circuit according to claim 1, wherein said insulation layer contains at least one substance selected from the group consisting of semiconductor oxides, semiconductor nitrides, fluorinated semiconductor oxides, fluorinated (amorphous) carbon, nitrides including boron nitride, polymers and polymer compounds including polyimides, polystyrenes, polyethylenes, polycarbonates, polybenzoxazole (PBO), benzocyclobutene (BCB), parylene, and fluoropolymers.

Claim 5 (original): The integrated electrical circuit according to claim 1, wherein said blocker layer contains one of nitrogen, oxygen, fluorine, and a compound thereof.

Claim 6 (original): The integrated electrical circuit according to claim 5, wherein said blocker layer contains a nitride.

Claim 7 (original): The integrated electrical circuit according to claim 6, wherein said blocker layer contains one of silicon nitride Si_3N_4 and tungsten silicon nitride WSi_xN.

Claim 8 (original): The integrated electrical circuit according to claim 5, wherein said blocker layer contains an oxidized nitride.

Claim 9 (original): The integrated electrical circuit according to claim 8, wherein said blocker layer contains at least one compound selected from the group consisting of silicon oxynitride SiON, silicon boron oxynitride SiBON, titanium oxynitride TiN_xO_y, tantalum oxynitride TaN_xO_y, and tungsten oxynitride WN_xO_y.

Claim 10 (original): The integrated electrical circuit according to claim 5, wherein said blocker layer contains a fluorinated nitride.

Claim 11 (original): The integrated electrical circuit as claimed in claim 10, wherein said blocker layer contains silicon fluorooxynitride SiOFN.

Claim 12 (original): The integrated electrical circuit according to claim 5, wherein said blocker layer contains a metal oxide.

Claim 13 (original): The integrated electrical circuit according to claim 5, wherein said blocker layer contains a material selected from the group consisting of titanium oxide TiO_2 and tantalum oxide Ta_2O_5.

Claim 14 (original): The integrated electrical circuit according to claim 1, wherein said blocker layer has a thickness of between 50 nm and 800 nm.

Claim 15 (original): The integrated electrical circuit according to claim 1, wherein said blocker layer is one of a plurality of blocker layers.

Claim 16 (original): The integrated electrical circuit according to claim 15, wherein said blocker layers are disposed on different ones of said structure planes.

Claim 17 (original): The integrated electrical circuit according to claim 15, wherein an extent to which said blocker layers impede diffusion and prevent diffusion differs.

Claim 18 (original): The integrated electrical circuit according to claim 1, including at least one further diffusion blocker bearing on at least a portion of said electrical connecting leads.

Claim 19 (original): The integrated electrical circuit according to claim 18, wherein said further diffusion blocker bears on at least one of side areas and lower edges of said portion of said electrical connecting leads.

Claim 20 (previously presented): The integrated electrical circuit according to claim 18, wherein said further diffusion blocker prevents bulk outdiffusion of copper into said first insulation layer.

Claim 21 (original): The integrated electrical circuit according to claim 18, wherein an extent to which said blocker layer impedes diffusion is greater than that of said further diffusion blocker.

Claim 22 (original): The integrated electrical circuit according to claim 18, wherein said blocker layer has a thickness greater than that of said further diffusion blocker.

Claim 23 (original): The integrated electrical circuit according to claim 18, wherein a diffusion through said blocker layer is less than 10% of a diffusion through said further diffusion blocker.

Claim 24 (withdrawn - currently amended): A method for fabricating an integrated electrical circuit, which comprises:

forming a plurality of structure planes including at least one element structure plane;

forming electrically active elements ~~in a region of a surface of a semiconductor substrate~~ on the at least one element structure plane;

applying a first insulation layer above the at least one element structure plane, the first insulation layer having first contact holes disposed therein, and the first contact holes being filled with a metal;

applying a second insulation layer above the first insulation layer, the second insulation layer having second contact holes disposed therein and filled with electrical connecting leads, and the second contact holes being further filled with copper in a whole-area manner;

applying connection pieces underneath the electrical connecting leads and above the first contact holes;

applying at least one diffusion blocker underneath the electrical connecting leads, the diffusion blocker at least one of impeding and preventing a diffusion of copper, the diffusion blocker configured as a blocker layer interrupted only in a region having the first contact holes formed therein, the blocker layer disposed between the first insulation layer and the second insulation layer; and

wherein the connection pieces are made of aluminum and cover the first contact holes and contact the connection leads, and the connection pieces are covered by the second insulation layer.

~~applying at least one diffusion blocker as a continuous blocker layer on the electrically active elements;~~

~~subsequently, applying at least one insulation layer on the continuous blocker layer; and~~

~~forming copper-containing electrical connecting leads at least one of within and on the insulation layer.~~

Claims 25-26 (canceled).

Claim 27 (previously presented): The integrated electrical circuit according to claim 1, wherein said blocker layer includes an upper surface facing said second insulation layer and a lower surface facing said structure plane, said connection pieces being in contact with said upper surface of said blocker layer.

Claim 28 (withdrawn - currently amended): The integrated electrical circuit according to claim 1, wherein said blocker layer includes an upper surface facing said ~~isolation~~ second insulation layer and a lower surface facing said structure plane, said connection pieces being in contact with said lower surface of said blocker layer.